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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,820	12/30/2003	Robert Allen Drehmel	00911.002700.1	1315
47213	7590	02/14/2005	EXAMINER	
FITZPATRICK CELLA (IBM) 30 ROCKEFELLER PLAZA NEW YORK, NY 10112-3800			VERBRUGGE, KEVIN	
			ART UNIT	PAPER NUMBER
			2188	

DATE MAILED: 02/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/747,820	DREHMEL ET AL.
	Examiner	Art Unit
	Kevin Verbrugge	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 18 January 2005.
2a) This action is FINAL. 2b) This action is non-final.
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-59 is/are pending in the application.
4a) Of the above claim(s) 11-59 is/are withdrawn from consideration.

5) Claim(s) 1-10 is/are allowed.

6) Claim(s) _____ is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 20 December 2003 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

DETAILED ACTION

Election/Restriction

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-10, drawn to a computer system, method, and processor, classified in class 710, subclass 306.

- II. Claims 11-59, drawn to a memory system, classified in class 711, subclass 5.

Invention I is directed to a computer system, method, and processor, all of which use a command bus and repeaters to broadcast a command such that the command is sent to the repeater using a plurality of bus cycles on a narrow bus while the repeater sends the command on using a single cycle on a wide bus. This arrangement is shown to "provide an enhanced processor-to-memory communication path for a multiprocessor computer system," "support an increased number of processors in a multiprocessor computer system," and "reduce the number of I/O pins and other hardware required to support communications in a multiprocessor system" (see U.S. Patent 6,526,469, claims 1, 7, and 10, and column 3, lines 25-36).

Invention II is directed to memory system architectures (also called interconnect topologies) which include a controller communicating to buffered memory modules (also

called memory subsystems) via point-to-point links (as opposed to a single bus shared by all memory modules) to eliminate physical interdependence between memory modules (or memory subsystems) (see U.S. Patent 6,502,161, claims 1, 10, 19, and 23, and the abstract and column 3, lines 47-55). This memory system architecture enables the memory system to “be upgraded by coupling additional memory module(s), each via a dedicated point-to-point link to the controller. Bandwidth may scale upwards as the memory system is upgraded by the additional memory module(s)” (column 3, lines 55-60).

In summary, the invention of U.S. Patent 6,526,469 enables adding more processors to a given amount of memory (by coalescing command pieces received in plural bus cycles into a single command transmitted in a single cycle), while the invention of U.S. Patent 6,502,161 enables adding more memory modules to a given processing entity (by providing a separate point-to-point bus between each memory module and the memory controller).

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as in a device where the memory controller is connected to a bus shared by plural memory subsystems (where the memory controller is not connected to the memory

devices using point to point links). Additionally, invention II has separate utility such as in a system where commands are always transmitted in a single cycle on full-width buses. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

Elected claims

Per MPEP 1450, claims 1-10 (Group I) are constructively elected and are herein treated on the merits.

Non-elected Claims

Per MPEP 1450, claims 11-59 (Group II) are constructively non-elected and withdrawn from consideration.

Allowable Subject Matter

Claims 1-10 are allowed.

Conclusion

This application is in condition for allowance except for the presence of claims 11-59. A complete reply to this action must include cancelation of the withdrawn claims or other appropriate action (37 CFR 1.144).

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

Any inquiry concerning a communication from the Examiner should be directed to the Examiner by phone at (571) 272-4214.

Any response to this action should be labeled appropriately (serial number, Art Unit 2188, and After-Final, Official, or Draft) and mailed to Commissioner for Patents, Washington, D.C. 20231 or faxed to (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.

A handwritten signature in black ink, appearing to read "Kevin Verbrugge". The signature is fluid and cursive, with a large, stylized "K" at the beginning.

Kevin Verbrugge
Primary Examiner
Art Unit 2188